

International Application No.: PCT/JP2005/009779

U.S. Patent Application No.: Unknown

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IN THE ABSTRACT:

Please replace the Abstract of the Disclosure originally filed with the above-identified patent application with the following new Abstract of the Disclosure:

ABSTRACT OF THE DISCLOSURE

In a manufacturing process of electronic components which include conductive patterns laminated with insulating layers provided therebetween, conductive pattern layers having conductive patterns formed at intervals therebetween along layer surfaces and insulating layers are alternately laminated to each other. The laminate is pressed by applying a force thereto in the lamination direction, followed by cutting of the laminate along cutting lines provided along boundaries between the electronic components, so that the electronic components are separated from each other. In a cutting-removal region of a mother substrate from which the electronic components are separated from each other by cutting, removal dummy patterns having a size allowing it to be disposed within the above region are formed. In the electronic component, floating dummy patterns which are not electrically connected to the conductive patterns are formed at intervals from the cutting-removal region.